What is Claimed is:

1. A method for characterizing a fault in an integrated circuit device, the integrated circuit device comprising primary inputs, primary outputs, and a plurality of signal lines and circuits interconnecting the primary inputs and outputs, the method comprising:

defining a fault tuple including an identification of a signal line, a signal line value, and a clock cycle constraint for the signal line such that the fault tuple is satisfied by providing a test sequence comprising one or more test patterns such that the signal line is controlled to the signal line value during a clock cycle of the test sequence defined by the clock cycle constraint responsive to application of the test sequence to the primary inputs.

2. A method according to Claim 1 further comprising:

defining a second fault tuple including an identification of a second signal line, a second signal line value, and a second clock cycle constraint for the second signal line such that a product of fault tuples includes the first and second fault tuples wherein the product of fault tuples is satisfied by providing the test sequence comprising one or more test patterns such that each of the signal lines of each of the fault tuples is controlled to the respective signal line values during clock cycles of the test sequence defined by the respective clock cycle constraints responsive to application of the test sequence to the primary inputs.

3. A method according to Claim 2 wherein at least one of the first and second signal line values comprises an error discrepancy wherein the product is detected when each fault tuple of the product is satisfied by providing the test sequence and the error discrepancy is observable at a primary output.

4. A method according to Claim 3 further comprising:

defining third and fourth fault tuples such that a second product of the third and fourth fault tuples is satisfied by providing a second test sequence comprising one or more test patterns wherein a macrofault comprising the first and second products

can be detected when either the first product or the second product is satisfied and a resulting error discrepancy is observable at a primary output.

5. A method according to Claim 2 further comprising:

generating a test sequence comprising a plurality of test patterns wherein the test sequence satisfies the first and second fault tuples of the product and wherein at least one of the first and second signal line values comprises an error discrepancy and wherein the error discrepancy is observable at a primary output in response to application of the test sequence to the primary inputs.

6. A method according to Claim 5 further comprising:

determining if the test sequence satisfies a second product of fault tuples representing a second fault to be characterized.

7. A method according to Claim 2 further comprising:

providing a test sequence comprising a plurality of test patterns; and

determining if the test sequence satisfies the product including the first and second fault tuples.

8. A method according to Claim 2 wherein the second clock cycle constraint is related to the first clock cycle constraint by an arithmetic or relational operator.

9. A method according to Claim 8 wherein the first fault tuple comprises a reference tuple.

10. A method of generating test patterns for an integrated circuit device, the integrated circuit comprising primary inputs, primary outputs, and a plurality of signal lines and circuits interconnecting the primary inputs and outputs, said method comprising:

providing at least one fault tuple including an identification of a signal line, a signal line value, and a clock cycle constraint for the signal line; and

determining a test sequence comprising at least one test pattern that can be applied to the primary inputs of the integrated circuit device to control the signal line to the signal line value during a clock cycle of the test sequence defined by the clock cycle constraint.

11. A method according to Claim 10:

wherein providing at least one fault tuple further comprises defining a second fault tuple including a second identification of a signal line, a second signal line value, and a second clock cycle constraint for the second signal line wherein a product comprises the first and second fault tuples; and

wherein determining a test sequence further comprises determining a test sequence that can be applied to the primary inputs of the integrated circuit device to control the first signal line to the first signal line value during the first clock cycle of the test sequence defined by the first clock cycle constraint and to control the second signal line to the second signal line value during a second clock cycle of the test sequence defined by the second clock cycle constraint.

12. A method according to Claim 11 wherein at least one of the first and second signal line values comprises an error discrepancy wherein determining the test sequence further comprises determining if the test sequence can manifest the error discrepancy at a primary output.

13. A method according to Claim 12 further comprising:

providing third and fourth fault tuples of a second product of fault tuples; and

wherein if the test sequence cannot manifest the error discrepancy at a primary output, determining a second test sequence that can be applied to the primary inputs of the integrated circuit device to satisfy the third and fourth fault tuples.

14. A method according to Claim 11 further comprising:

determining if the test sequence satisfies a second product of fault tuples representing a second fault to be characterized.

15. A method according to Claim 11 wherein the second clock cycle constraint is related to the first clock cycle constraint by an arithmetic or relational operator.

16. A method according to Claim 15 wherein the first fault tuple comprises a reference tuple.

17. A method of simulating a test pattern for an integrated circuit device, the integrated circuit device comprising primary inputs, primary outputs, and a plurality of signal lines and circuits interconnecting the primary inputs and outputs, the method comprising:

providing a fault tuple including an identification of a signal line, a signal line value, and a clock cycle constraint for the signal line;

providing a test sequence comprising one or more test patterns; and

determining if the fault tuple will be satisfied by the test pattern such that the signal line is controlled to the signal line value during a clock cycle of the test sequence defined by the clock cycle constraint responsive to application of the test sequence to the primary inputs.

18. A method according to Claim 17 further comprising:

providing a second fault tuple including an identification of a second signal line, a second signal line value, and a second clock cycle constraint for the second signal line such that a product of fault tuples includes the first and second fault tuples; and

determining if the second fault tuple will be satisfied by the test pattern such that the second signal lines is controlled to the second signal line value during a clock cycle of the test sequence defined by the second clock cycle constraint responsive to application of the test sequence to the primary inputs.

19. A method according to Claim 18 wherein at least one of the first and second signal line values comprises an error discrepancy, the method further comprising:

determining if the error discrepancy will be observable at a primary output responsive to application of the test sequence to the primary inputs.

20. A method according to Claim 18 further comprising:

if the first and second fault tuples will not be satisfied by the test pattern or if the error discrepancy will not be not be observable at a primary output, generating a second test sequence comprising a plurality of test patterns wherein the test sequence satisfies the first and second fault tuples of the product and wherein at least one of the first and second signal line values comprises an error discrepancy and wherein the error discrepancy is observable at a primary output in response to application of the second test sequence to the primary inputs.

21. A method according to Claim 20 further comprising:

determining if the second test sequence satisfies a second product of fault tuples representing a second fault to be characterized.

22. A method according to Claim 18 wherein the second clock cycle constraint is related to the first clock cycle constraint by an arithmetic or relational operator.

23. A method according to Claim 22 wherein the first fault tuple comprises a reference tuple.

24. A system for generating test patterns for an integrated circuit device, the integrated circuit comprising primary inputs, primary outputs, and a plurality of signal lines and circuits interconnecting the primary inputs and outputs, said system comprising:

means for providing at least one fault tuple including an identification of a signal line, a signal line value, and a clock cycle constraint for the signal line; and

means for determining a test sequence comprising at least one test pattern that can be applied to the primary inputs of the integrated circuit device to control the signal line to the signal line value during a clock cycle of the test sequence defined by the clock cycle constraint.

25. A system according to Claim 24:

wherein said means for providing at least one fault tuple further comprises means for defining a second fault tuple including a second identification of a signal line, a second signal line value, and a second clock cycle constraint for the second signal line wherein a product comprises the first and second fault tuples; and

wherein said means for determining a test sequence further comprises means for determining a test sequence that can be applied to the primary inputs of the integrated circuit device to control the first signal line to the first signal line value during the first clock cycle of the test sequence defined by the first clock cycle constraint and to control the second signal line to the second signal line value during a second clock cycle of the test sequence defined by the second clock cycle constraint.

26. A system according to Claim 25 wherein at least one of the first and second signal line values comprises an error discrepancy wherein said means for determining the test sequence further comprises means for determining if the test sequence can manifest the error discrepancy at a primary output.

27. A system according to Claim 26 further comprising:

means for providing third and fourth fault tuples of a second product of fault tuples; and

means for determining a second test sequence that can be applied to the primary inputs of the integrated circuit device to satisfy the third and fourth fault tuples if the test sequence cannot manifest the error discrepancy at a primary output.

28. A system according to Claim 25 further comprising:

means for determining if the test sequence satisfies a second product of fault tuples representing a second fault to be characterized.

29. A system according to Claim 25 wherein the second clock cycle constraint is related to the first clock cycle constraint by an arithmetic or relational operator.

30. A system according to Claim 29 wherein the first fault tuple comprises a reference tuple.

31. A system for simulating a test pattern for an integrated circuit device, the integrated circuit device comprising primary inputs, primary outputs, and a plurality of signal lines and circuits interconnecting the primary inputs and outputs, the system comprising:

means for providing a fault tuple including an identification of a signal line, a signal line value, and a clock cycle constraint for the signal line;

means for providing a test sequence comprising one or more test patterns; and

means for determining if the fault tuple will be satisfied by the test pattern such that the signal line is controlled to the signal line value during a clock cycle of the test sequence defined by the clock cycle constraint responsive to application of the test sequence to the primary inputs.

32. A system according to Claim 31 further comprising:

means for providing a second fault tuple including an identification of a second signal line, a second signal line value, and a second clock cycle constraint for the second signal line such that a product of fault tuples includes the first and second fault tuples; and

means for determining if the second fault tuple will be satisfied by the test pattern such that the second signal lines is controlled to the second signal line value during a clock cycle of the test sequence defined by the second clock cycle constraint responsive to application of the test sequence to the primary inputs.

33. A system according to Claim 32 wherein at least one of the first and second signal line values comprises an error discrepancy, the system further comprising:

means for determining if the error discrepancy will be observable at a primary output responsive to application of the test sequence to the primary inputs.

34. A system according to Claim 32 further comprising:

means for generating a second test sequence if the first and second fault tuples will not be satisfied by the first test sequence or if the error discrepancy will not be not be observable at a primary output, the second test sequence comprising a plurality of test patterns wherein the second test sequence satisfies the first and second fault tuples of the product and wherein at least one of the first and second signal line values comprises an error discrepancy and wherein the error discrepancy is observable at a primary output in response to application of the second test sequence to the primary inputs.

35. A system according to Claim 34 further comprising:

means for determining if the second test sequence satisfies a second product of fault tuples representing a second fault to be characterized.

36. A system according to Claim 32 wherein the second clock cycle constraint is related to the first clock cycle constraint by an arithmetic or relational operator.

37. A system according to Claim 36 wherein the first fault tuple comprises a reference tuple.

38. A computer program product for generating test patterns for an integrated circuit device, the integrated circuit comprising primary inputs, primary outputs, and a plurality of signal lines and circuits interconnecting the primary inputs and outputs, the computer program product comprising a computer-readable storage medium having computer-readable program code embodied in the medium, the computer-readable program code comprising:

computer-readable program code that provides at least one fault tuple including an identification of a signal line, a signal line value, and a clock cycle constraint for the signal line; and

computer-readable program code that determines a test sequence comprising at least one test pattern that can be applied to the primary inputs of the integrated circuit device to control the signal line to the signal line value during a clock cycle of the test sequence defined by the clock cycle constraint.

39. A computer program product according to Claim 38:

wherein the computer-readable program code that provides at least one fault tuple further provides a second fault tuple including a second identification of a signal line, a second signal line value, and a second clock cycle constraint for the second signal line wherein a product comprises the first and second fault tuples; and

wherein the computer-readable program code that determines a test sequence further determines a test sequence that can be applied to the primary inputs of the integrated circuit device to control the first signal line to the first signal line value during the first clock cycle of the test sequence defined by the first clock cycle constraint and to control the second signal line to the second signal line value during a second clock cycle of the test sequence defined by the second clock cycle constraint.

40. A computer program product according to Claim 39 wherein at least one of the first and second signal line values comprises an error discrepancy wherein the computer-readable program code that determines the test sequence further determines if the test sequence can manifest the error discrepancy at a primary output.

41. A computer program product according to Claim 40 further comprising:

computer-readable program code that provides third and fourth fault tuples of a second product of fault tuples; and

computer-readable program code that determines a second test sequence that can be applied to the primary inputs of the integrated circuit device to satisfy the third and fourth fault tuples if the first test sequence cannot manifest the error discrepancy at a primary output.

42. A computer program product according to Claim 39 further comprising:

computer-readable program code that determines if the test sequence satisfies a second product of fault tuples representing a second fault to be characterized.

43. A computer program product according to Claim 39 wherein the second clock cycle constraint is related to the first clock cycle constraint by an arithmetic or relational operator.

44. A computer program product according to Claim 43 wherein the first fault tuple comprises a reference tuple.

45. A computer program product for simulating a test pattern for an integrated circuit device, the integrated circuit device comprising primary inputs, primary outputs, and a plurality of signal lines and circuits interconnecting the primary inputs and outputs, the computer program product comprising a computer-readable storage medium having computer-readable program code embodied in the medium, the computer-readable program code comprising:

computer-readable program code that provides a fault tuple including an identification of a signal line, a signal line value, and a clock cycle constraint for the signal line;

computer-readable program code that provides a test sequence comprising one or more test patterns; and

computer-readable program code that determines if the fault tuple will be satisfied by the test pattern such that the signal line is controlled to the signal line value during a clock cycle of the test sequence defined by the clock cycle constraint responsive to application of the test sequence to the primary inputs.

46. A computer program product according to Claim 45 further comprising:

computer-readable program code that provides a second fault tuple including an identification of a second signal line, a second signal line value, and a second clock cycle constraint for the second signal line such that a product of fault tuples includes the first and second fault tuples; and

computer-readable program code that determines if the second fault tuple will be satisfied by the test pattern such that the second signal lines is controlled to the second signal line value during a clock cycle of the test sequence defined by the

second clock cycle constraint responsive to application of the test sequence to the primary inputs.

47. A computer program product according to Claim 46 wherein at least one of the first and second signal line values comprises an error discrepancy, the computer program product further comprising:

computer-readable program code that determines if the error discrepancy will be observable at a primary output responsive to application of the test sequence to the primary inputs.

48. A computer program product according to Claim 46 further comprising:

computer-readable program code that generates a second test sequence if the first and second fault tuples will not be satisfied by the test pattern or if the error discrepancy will not be not be observable at a primary output, the second test sequence comprising a plurality of test patterns wherein the test sequence satisfies the first and second fault tuples of the product and wherein at least one of the first and second signal line values comprises an error discrepancy and wherein the error discrepancy is observable at a primary output in response to application of the second test sequence to the primary inputs.

49. A computer program product according to Claim 48 further comprising:

computer-readable program code that determines if the second test sequence satisfies a second product of fault tuples representing a second fault to be characterized.

50. A computer program product according to Claim 46 wherein the second clock cycle constraint is related to the first clock cycle constraint by an arithmetic or relational operator.

51. A computer program product according to Claim 50 wherein the first fault tuple comprises a reference tuple.

52. A method of generating test patterns for an integrated circuit device, the integrated circuit device comprising primary inputs, primary outputs, and a plurality of signal lines and circuits interconnecting the primary inputs and outputs, said method comprising:

providing a list of a plurality of macrofaults each representing a respective possible fault condition of the integrated circuit device;

generating a first test sequence that can detect a first macrofault from the list;

simulating the first test sequence for macrofaults from the list to determine if any other macrofaults from the list can be detected using the first test sequence;

dropping any macrofaults from the list that can be detected using the first test sequence; and

generating a second test sequence that can detect a second macrofault from the list of remaining macrofaults.

53. A method according to Claim 52 wherein generating the first test sequence alternately comprises determining if a test sequence cannot be generated to detect the first macrofault, wherein simulating the first test sequence is omitted when a test sequence cannot be generate, and wherein dropping any macro faults comprises dropping the macrofault for which a test sequence cannot be generated.

54. A method according to Claim 53 wherein operations of generating, simulating, and dropping are repeated until all macrofaults have been dropped from the list.

55. A method according to Claim 53 wherein generating a first test sequence that can detect a first macrofault from the list comprises selecting the first macrofault from the list according to a heuristics based order.